AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A processor array, comprising an array of processor elements, wherein each of said processor elements comprises a modulo-n cycle counter, and wherein at least one of said processor elements is able to transmit control command signals to each of the other processor elements,

each processor element being such that, on receipt of a control command signal, it acts on that signal only when its cycle counter reaches a predetermined value, and

said one of said processor elements being such that it transmits control command signals only when its cycle counter takes a value which is within a predetermined range, said predetermined range being a subset smaller than a set of n possible values of the modulo-n cycle counter,

the processor array further comprising a first connection between each of said processor elements, wherein said one of said processor elements is able to transmit synchronization control command signals on said first connection, and wherein each processor element acts on a synchronization control command signal received on said first connection by restarting its cycle counter.

2. (Previously Presented) A processor array as claimed in claim 1, comprising a second connection between each of said processor elements, wherein said one of said processor elements is able to transmit start and stop control command signals on said first connection, and wherein each processor element acts on start and stop control command signals received on said first connection.

3. (Original) A processor array as claimed in claim 2, wherein a start control command signal comprises a first binary signal level on said first connection, and a stop control command signal comprises a second binary signal level on said first connection.

4. (Previously Presented) A processor array as claimed in claim 2, comprising a third connection between each of said processor elements, wherein each of said processor elements is able to place a halt request signal on said second connection, and said one of said processor elements detects any halt request signal placed on the second connection, and acts on a detected halt request signal by transmitting a stop control command signal on said first connection.

5. (Previously Presented) A processor array as claimed in claim 1, comprising a fourth connection between each of said processor elements, wherein said one of said processor elements is able to transmit step control command signals on said third connection, and wherein each processor element acts on a step

control command signal received on said third connection by performing one process step.

6. (Canceled)

7. (Original) A processor array as claimed in claim 1, wherein each processor element comprises a programmable delay line, for applying a programmed delay to received control command signals.

8. (Original) A processor array as claimed in claim 7, wherein each programmable delay line has a minimum programmable delay.

9. (Original) A processor array as claimed in claim 1, wherein said processor elements include a transmit element and a receive element, and wherein:

said transmit element comprises means for transmitting data words in association with respective code words, said code words being used in a predetermined sequence; and

said receive element comprises:

means for storing received data words in respective registers, the respective registers being determined on the basis of the code words associated with the data words, such that each received data word is stored in its respective register for the duration of said predetermined sequence of code words; and

means for retrieving data words from the respective registers.

10. (Original) A processor array as claimed in claim 9, wherein said means for retrieving data words from the respective registers comprises a multiplexer, connected to all of the registers, and means for selecting an output from each of the registers in turn.

11. (Currently Amended) A processor array, comprising an array of processor elements, wherein each of said processor elements comprises a modulo-n cycle counter, and wherein at least one of said processor elements is able to transmit control command signals to each of the other processor elements,

each processor element being such that, on receipt of a control command signal, it acts on that signal only when its cycle counter reaches a predetermined value, and

said one of said processor elements being such that it transmits control command signals only when its cycle counter takes a value which is within a predetermined range, said predetermined range being a subset smaller than a set of n possible values of the modulo-n cycle counter,

wherein said processor elements include a data transmit element and a data receive element, and wherein:

said data transmit element comprises means for transmitting data words in association with respective code words based on a transmit clock, said code words being used in a predetermined sequence; and

said receive element comprises:

a decoder, for deriving from signals received from a transmitting processor element a first clock corresponding to the transmit clock of the transmitting processor, and for storing received data words in respective registers based on the first clock, the respective registers being determined on the basis of the code words associated with the data words, such that each received data word is stored in its respective register for the duration of said predetermined sequence of code words; and

means for retrieving data words from the respective registers based on a receive clock.

12. (Currently Amended) A processor array, comprising an array of processor elements, wherein each of said processor elements comprises a modulo-n cycle counter, and wherein a first of said processor elements is able to transmit control command signals to each of the other processor elements,

each processor element being such that, on receipt of a control command signal, it acts on that signal only when its cycle counter reaches a predetermined value, and

said first of said processor elements being such that it transmits control command signals only when its cycle counter takes a value which is within a predetermined range, said predetermined range being a subset smaller than a set of n possible values of the modulo-n cycle counter,

the processor array further comprising:

a start and stop control connection between each of said processor elements, wherein said first of said processor elements is able to transmit start and stop control command signals on said start and stop control connection, and wherein each processor element acts on start and stop control command signals received on said start and stop control connection; and

a halt connection between each of said processor elements, wherein each of said processor elements is able to place a halt request signal on said halt connection, and said first of said processor elements detects any halt request signal placed on the halt connection, and acts on a detected halt request signal by transmitting a stop control command signal on said start and stop control connection.

13. (New) The processor array of claim 1, wherein each processor element acts on the control command signal only during a time when its cycle counter holds the predetermined value.

14. (New) The processor array of claim 11, wherein each processor element acts on the control command signal only during a time when its cycle counter holds the predetermined value.

15. (New) The processor array of claim 12, wherein each processor element acts on the control command signal only during a time when its cycle counter holds the predetermined value.